# Vivado FPGA Design Flow on Zynq Ultrascale+

This workshop shows how to develop digital designs in Xilinx FPGA fabric.

The labs have been developed on a PC running Microsoft Windows 10 professional edition and using Vivado 2022.1.

# Supported Boards

ZCU106 Zynq UltraScale+ MPSoC board

# Lab source files

All the source files are located in {this\_repository}/source folder.

For the ZCU106 board, when creating Vivado projects, select Boards tab and then select Zynq UltraScale+ ZCU106 MPSoC Evaluation Platform

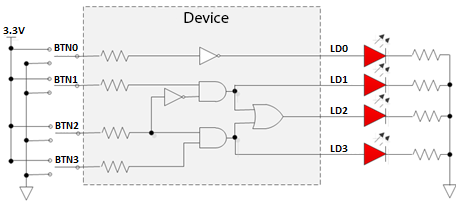
# Hardware Setup

**Zynq UltraScale+ MPSoC:** Connect the platform to the PC with two micro-USB cables. Connect the micro-USB cable to the port labeled "USB UART" and "USB JTAG". Turn on your kit by moving the power switch in the bottom-right corner to the On position. You will see many Green LEDs and a small fan run when switch powers on. The kit needs to be connected to a full power USB port to operate correctly.

# Labs Overview:

**Lab 1**

This lab guides you through the process of using the Vivado IDE to create a simple HDL design. You will simulate the design with built-in Vivado XSim simulator.



**Lab 2**

This lab guides you through the process of using the Vivado IDE to package the design you created in lab 1 with the Vivado IP packager. You will add a AXI-Lite Slave Interface to the design you created in lab 1 and will use the VIP Ips to simulate the packaged IP.

**Lab 3**

This lab guides you through the process of using Vivado to Synthesis, Implement, Generate the bitstream and program the FPGA for the design you created in lab 1. You will also perform Post-Implementation Simulation.

**Lab 4**

This lab guides you through the process of creating a completed Embedded Platform with the Zynq MpSoC Platform. You will make add some general GPIO IPs from Xilinx to control the input/output peripherals on the board. You may also add the IP from lab 2 to the hardware system

**Lab 5**

This lab guides you through the process of using Vitis IDE to create a software platform and write bare-metal applications to run with the hardware platform you created in lab 4.